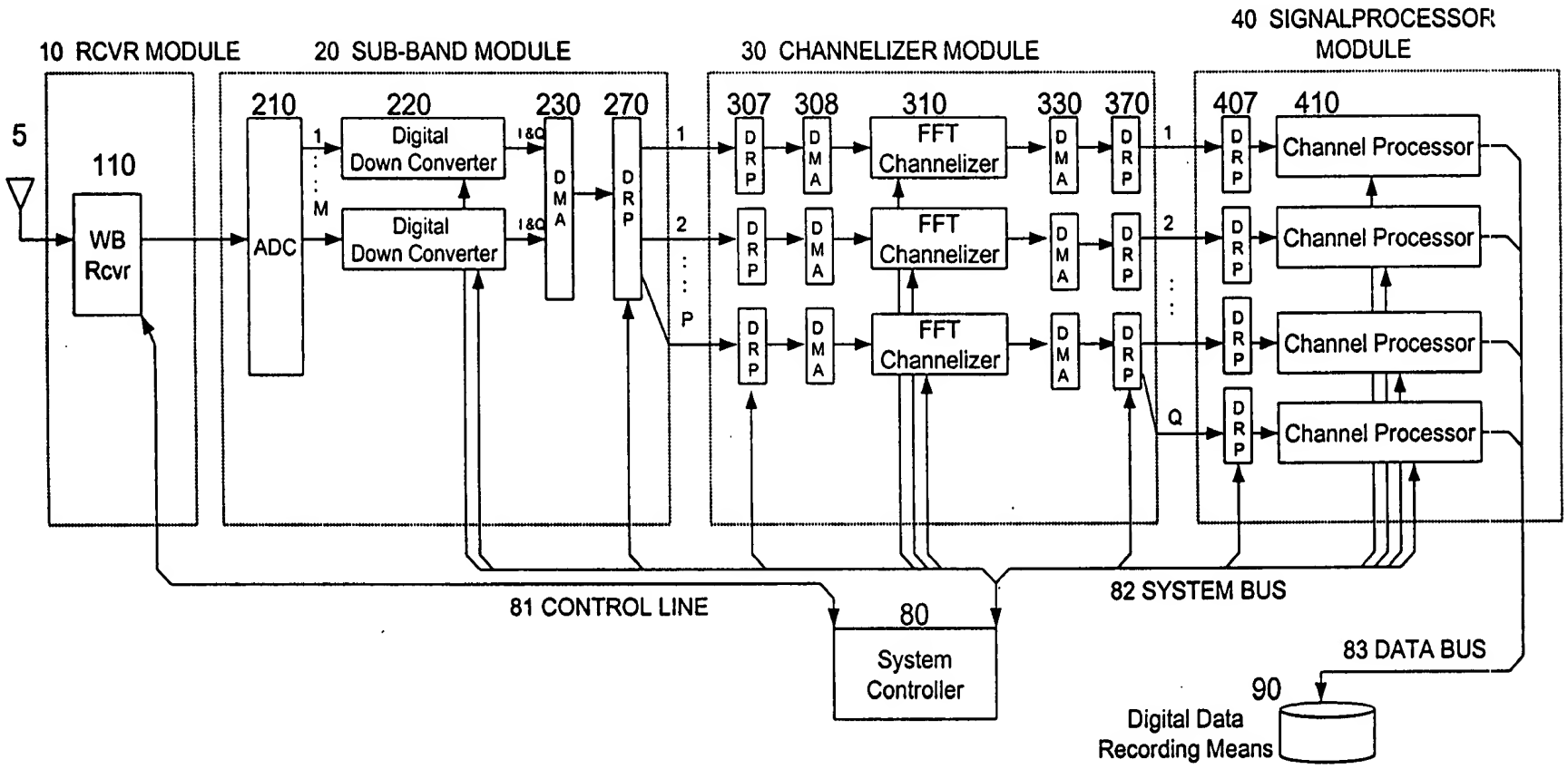


Fig. 1a

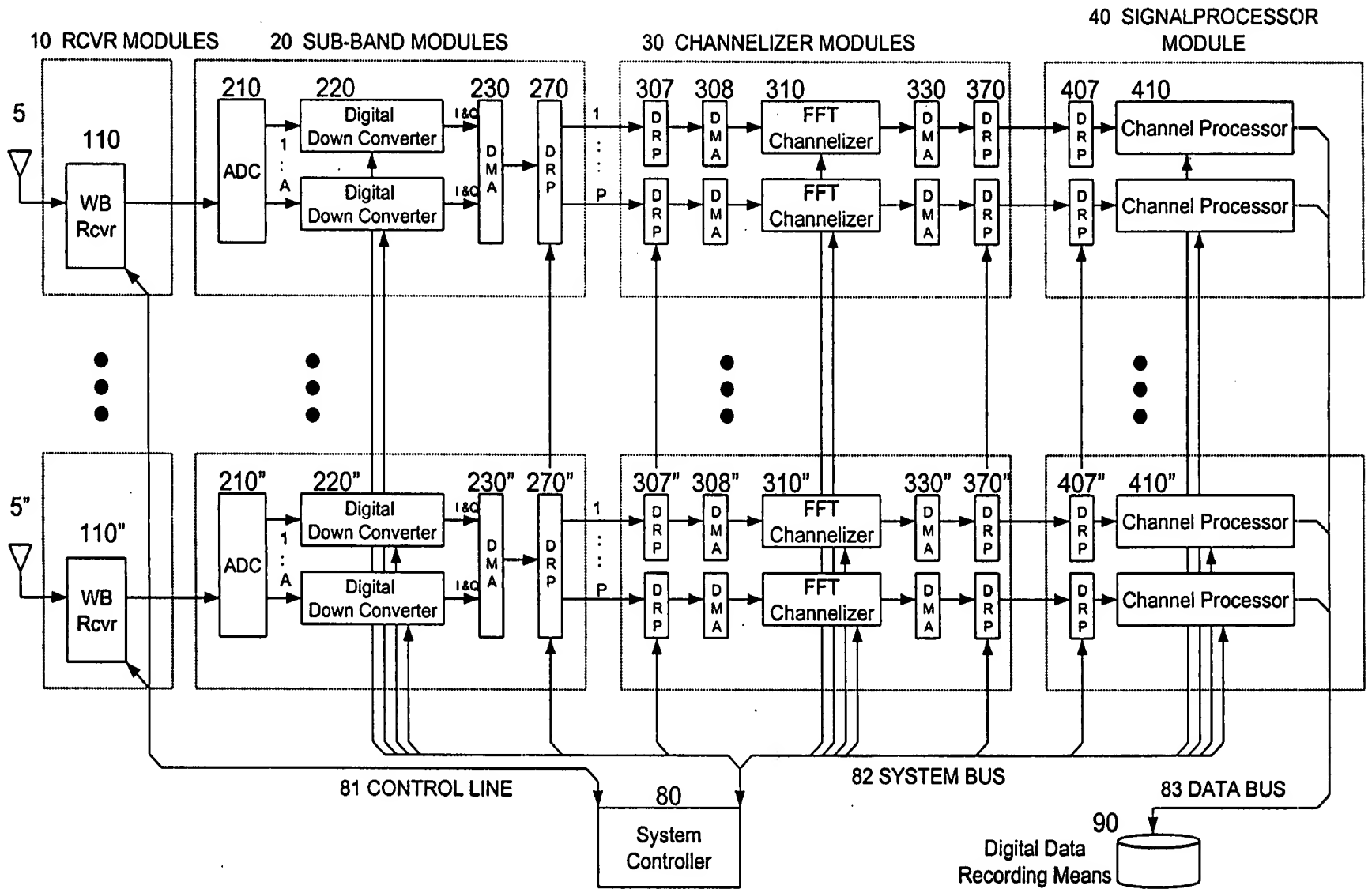

10 RCVR MODULES
20 SUB-BAND MODULES
30 CHANNELIZER MODULES
40 SIGNALPROCESSOR MODULE
5
110
WB Rcvr
210
ADC
1
A
220
Digital Down Converter
Digital Down Converter
I&Q
230
DMA
270
DRP
1
P
307
308
310
FFT Channelizer
330
370
407
410
Channel Processor
5"
110"
210"
220"
230"
270"
307"
308"
310"
330"
370"
407"
410"
81 CONTROL LINE
80
System Controller
82 SYSTEM BUS
83 DATA BUS
90
Digital Data Recording Means

Fig. 1b

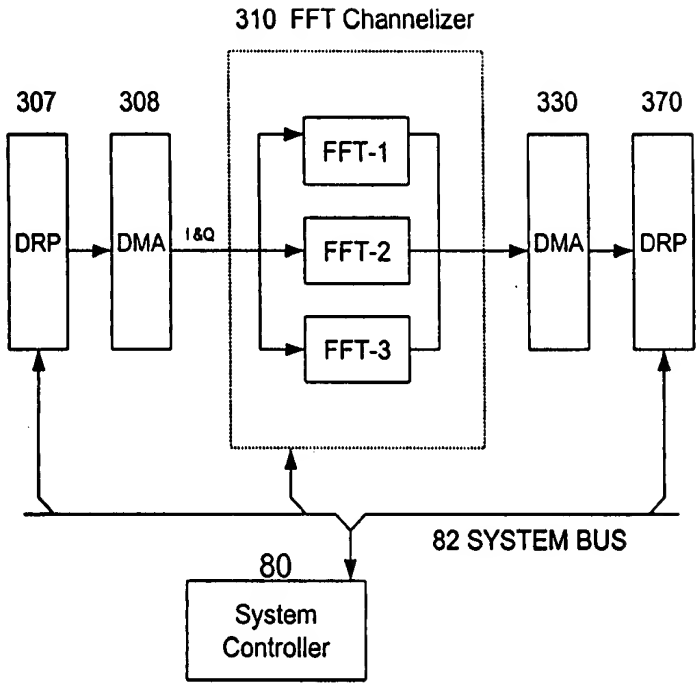


Fig. 2a

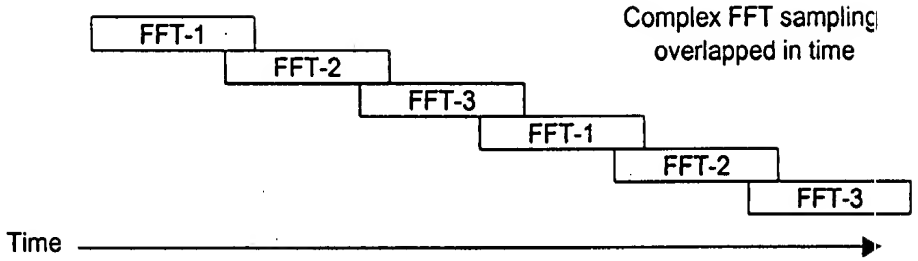


Fig. 2b

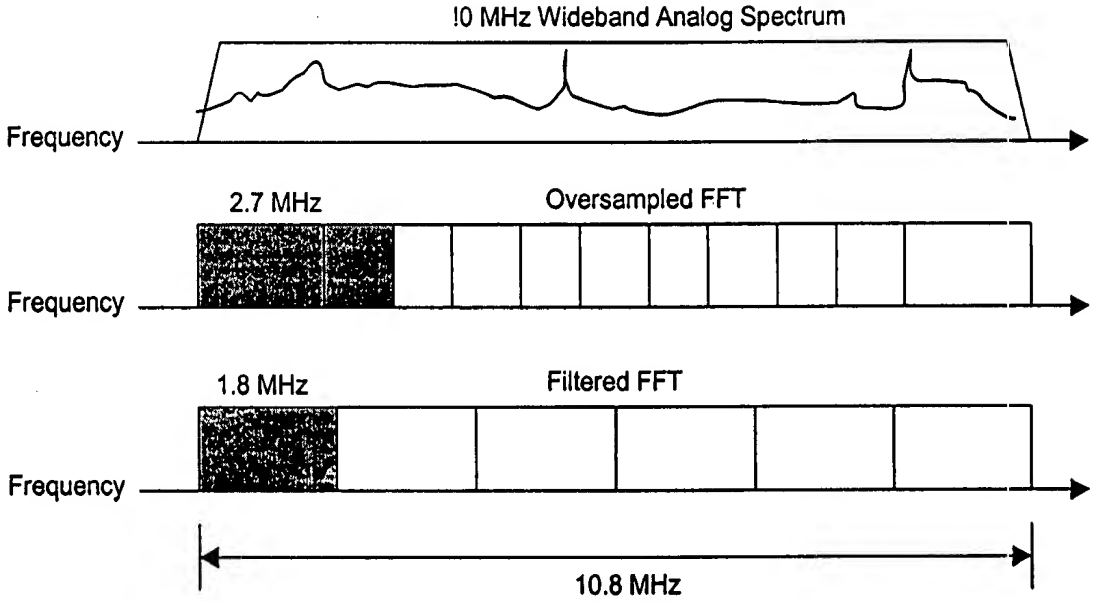


Fig. 2c

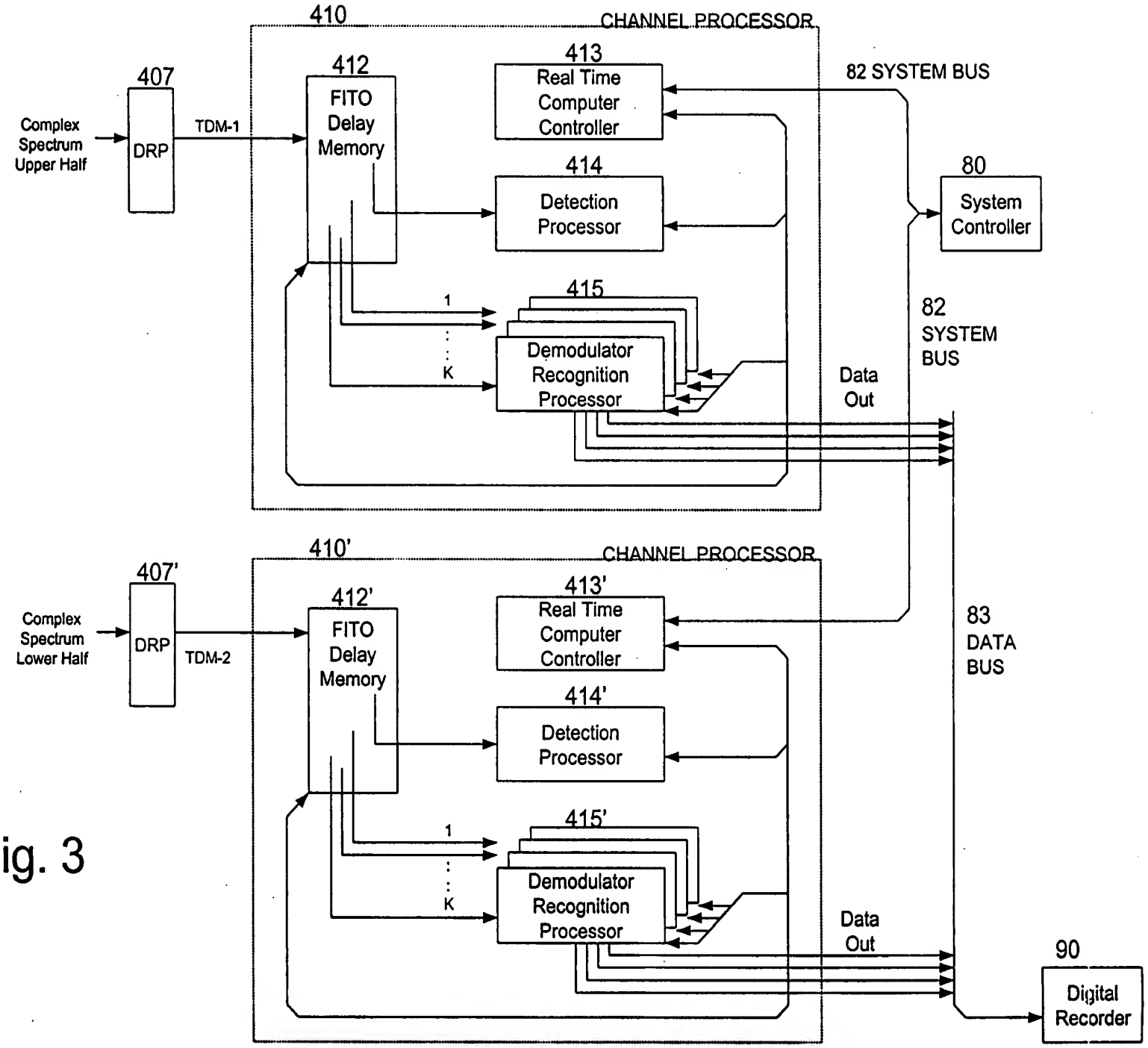

410
CHANNEL PROCESSOR
412
FITO
Delay
Memory
413
Real Time
Computer
Controller
82 SYSTEM BUS
407
Complex
Spectrum
Upper Half
DRP
TDM-1
414
Detection
Processor
80
System
Controller
415
1
K
Demodulator
Recognition
Processor
82
SYSTEM
BUS
Data
Out
410'
CHANNEL PROCESSOR
407'
412'
FITO
Delay
Memory
413'
Real Time
Computer
Controller
Complex
Spectrum
Lower Half
DRP
TDM-2
83
DATA
BUS
414'
Detection
Processor
415'
1
K
Demodulator
Recognition
Processor
Data
Out
90
Digital
Recorder

Fig. 3

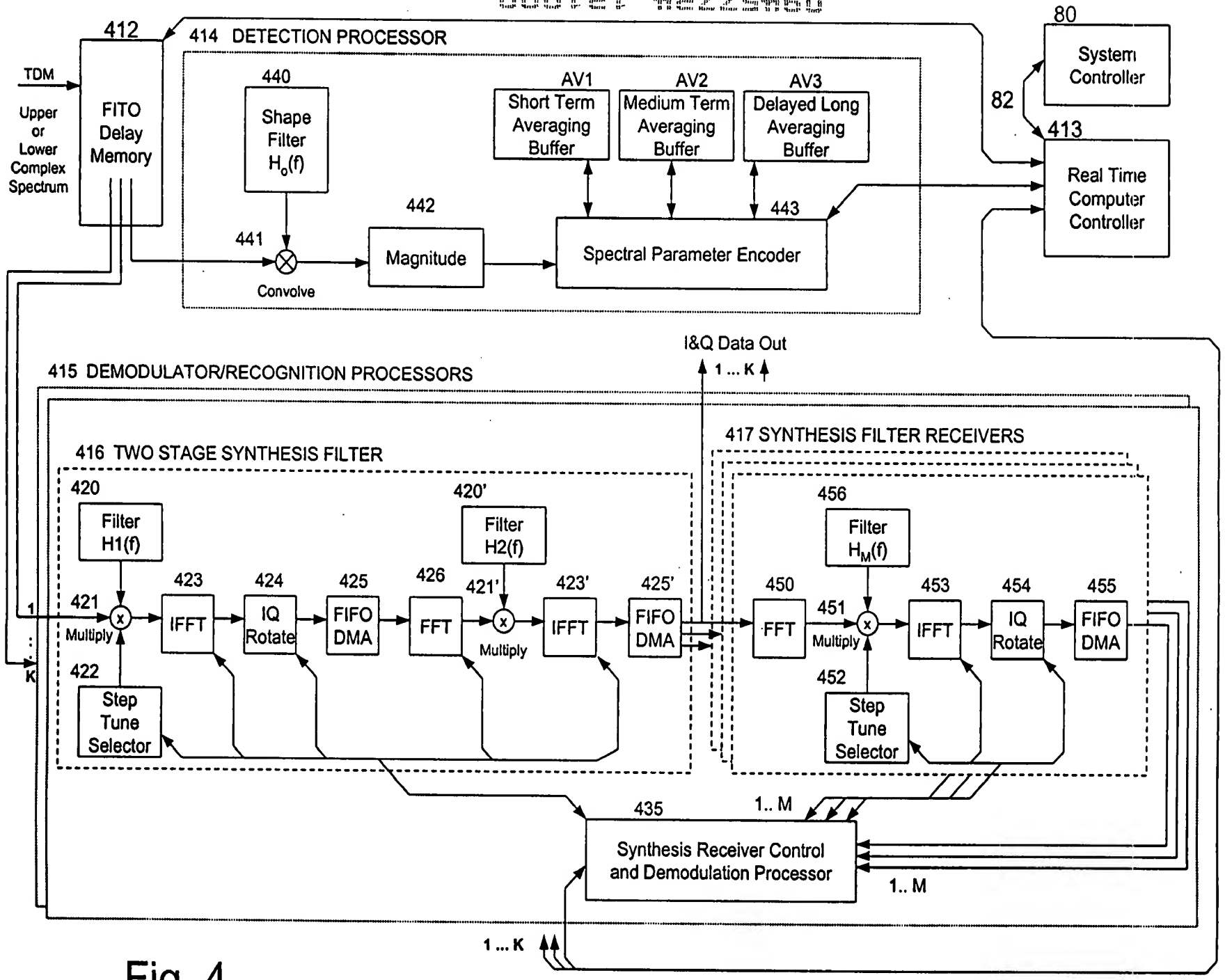

412
414 DETECTION PROCESSOR
80
System Controller
82
413
Real Time Computer Controller
TDM
Upper or Lower Complex Spectrum
FITO Delay Memory
440
Shape Filter $H_o(f)$
AV1
Short Term Averaging Buffer
AV2
Medium Term Averaging Buffer
AV3
Delayed Long Averaging Buffer
441
Convolve
442
Magnitude
443
Spectral Parameter Encoder
I&Q Data Out
1 ... K
415 DEMODULATOR/RECOGNITION PROCESSORS
416 TWO STAGE SYNTHESIS FILTER
417 SYNTHESIS FILTER RECEIVERS
420
Filter H1(f)
420'
Filter H2(f)
456
Filter $H_M(f)$
421
Multiply
423
IFFT
424
IQ Rotate
425
FIFO DMA
426
FFT
421'
Multiply
423'
IFFT
425'
FIFO DMA
450
FFT
451
Multiply
453
IFFT
454
IQ Rotate
455
FIFO DMA
422
Step Tune Selector
452
Step Tune Selector
435
1.. M
Synthesis Receiver Control and Demodulation Processor
1.. M
1 ... K

Fig. 4

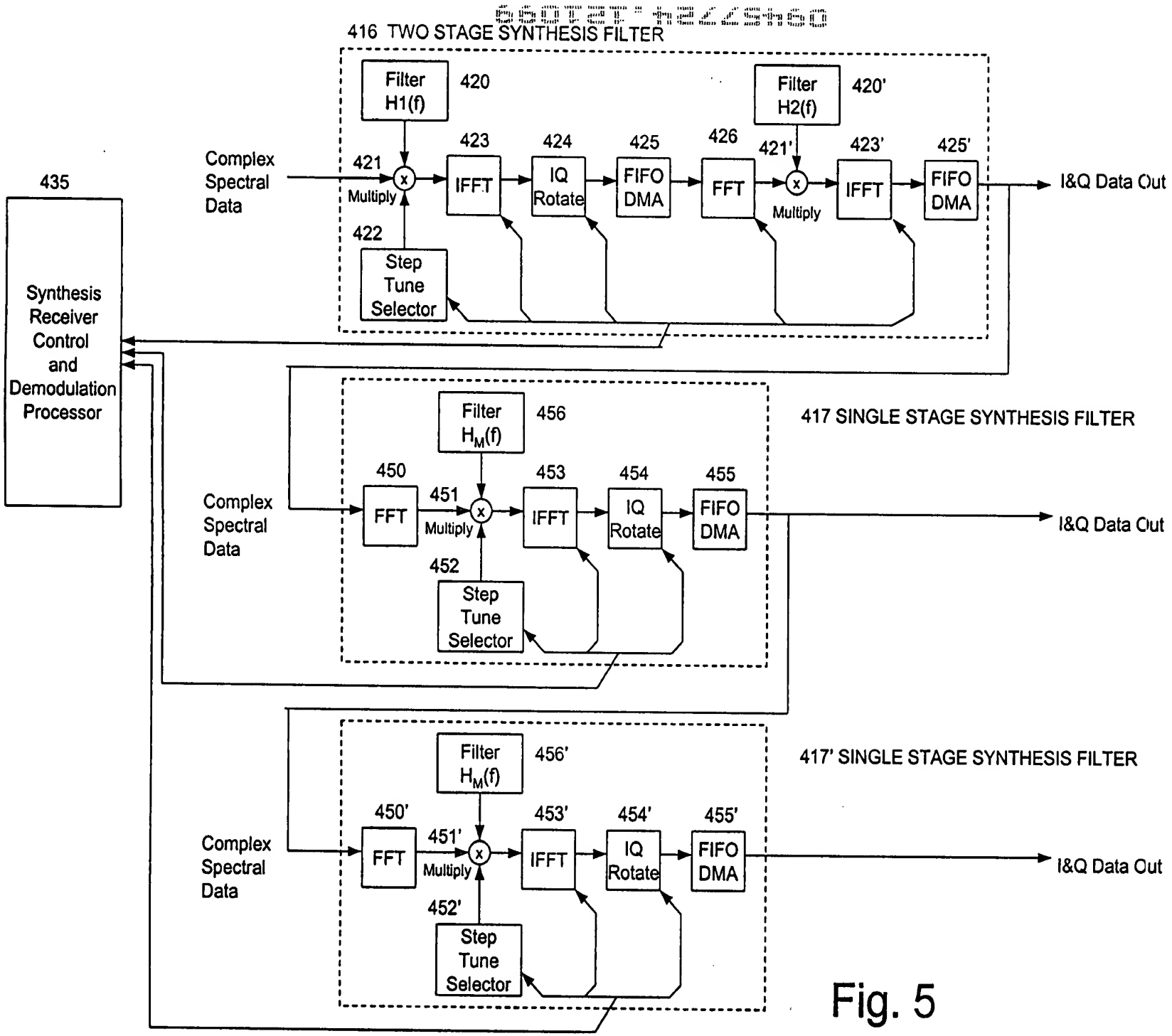

416 TWO STAGE SYNTHESIS FILTER
Filter H1(f)
420
Filter H2(f)
420'
Complex Spectral Data
421
423
424
425
426
421'
423'
425'
Multiply
IFFT
IQ Rotate
FIFO DMA
FFT
Multiply
IFFT
FIFO DMA
I&Q Data Out
422
Step Tune Selector
435
Synthesis Receiver Control and Demodulation Processor
417 SINGLE STAGE SYNTHESIS FILTER
Filter $H_M(f)$
456
Complex Spectral Data
450
451
453
454
455
FFT
Multiply
IFFT
IQ Rotate
FIFO DMA
I&Q Data Out
452
Step Tune Selector
417' SINGLE STAGE SYNTHESIS FILTER
Filter $H_M(f)$
456'
Complex Spectral Data
450'
451'
453'
454'
455'
FFT
Multiply
IFFT
IQ Rotate
FIFO DMA
I&Q Data Out
452'
Step Tune Selector

Fig. 5

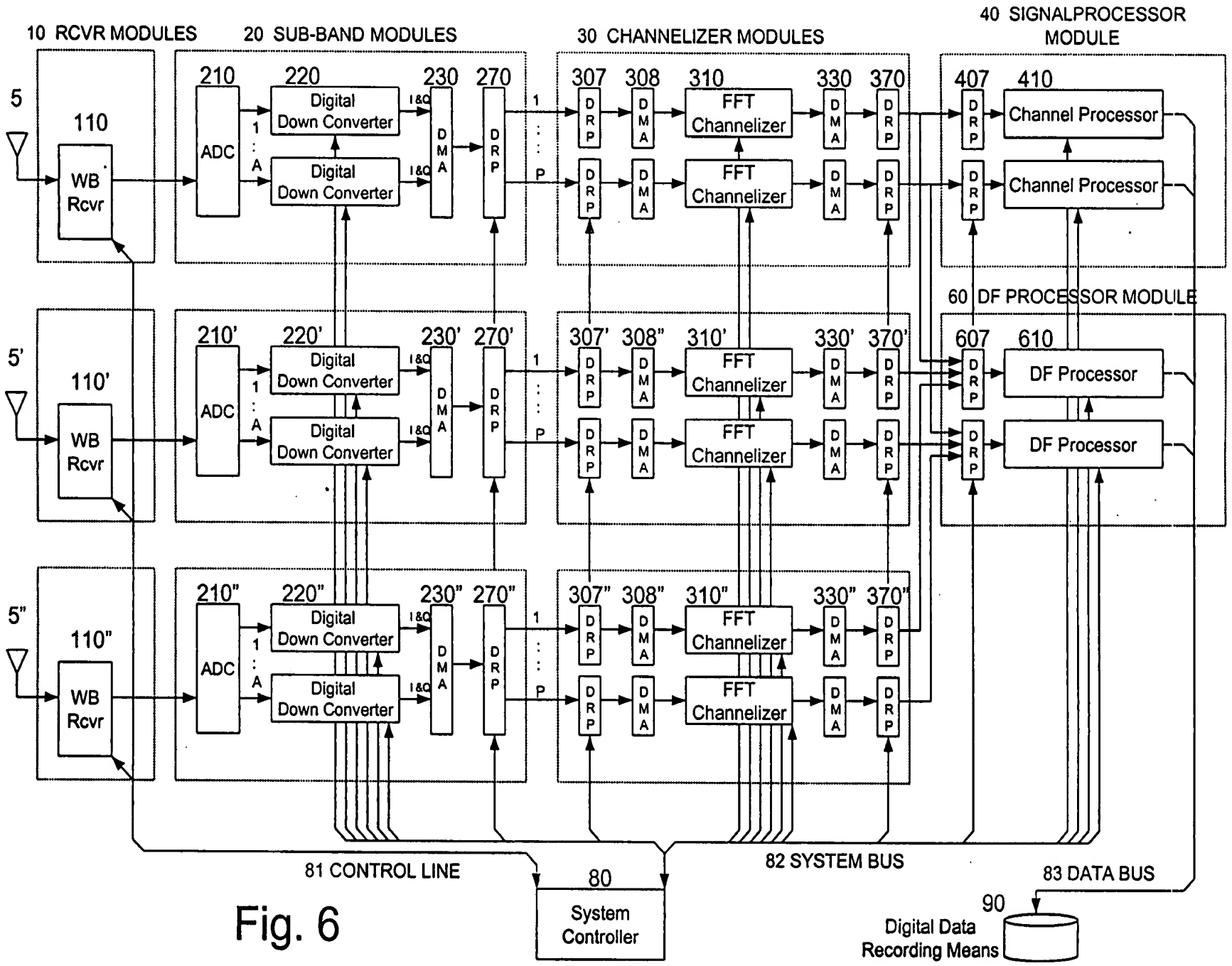

10 RCVR MODULES
20 SUB-BAND MODULES
30 CHANNELIZER MODULES
40 SIGNALPROCESSOR MODULE
60 DF PROCESSOR MODULE
5
110
WB Rcvr
ADC
1 : A
210
220
Digital Down Converter
I&Q
230
DMA
270
DRP
1 : P
307
308
310
FFT Channelizer
330
370
407
410
Channel Processor
607
610
DF Processor
5'
110'
210'
220'
230'
270'
307'
308"
310'
330'
370'
5"
110"
210"
220"
230"
270"
307"
308"
310"
330"
370"
81 CONTROL LINE
80
System Controller
82 SYSTEM BUS
83 DATA BUS
90
Digital Data Recording Means

Fig. 6

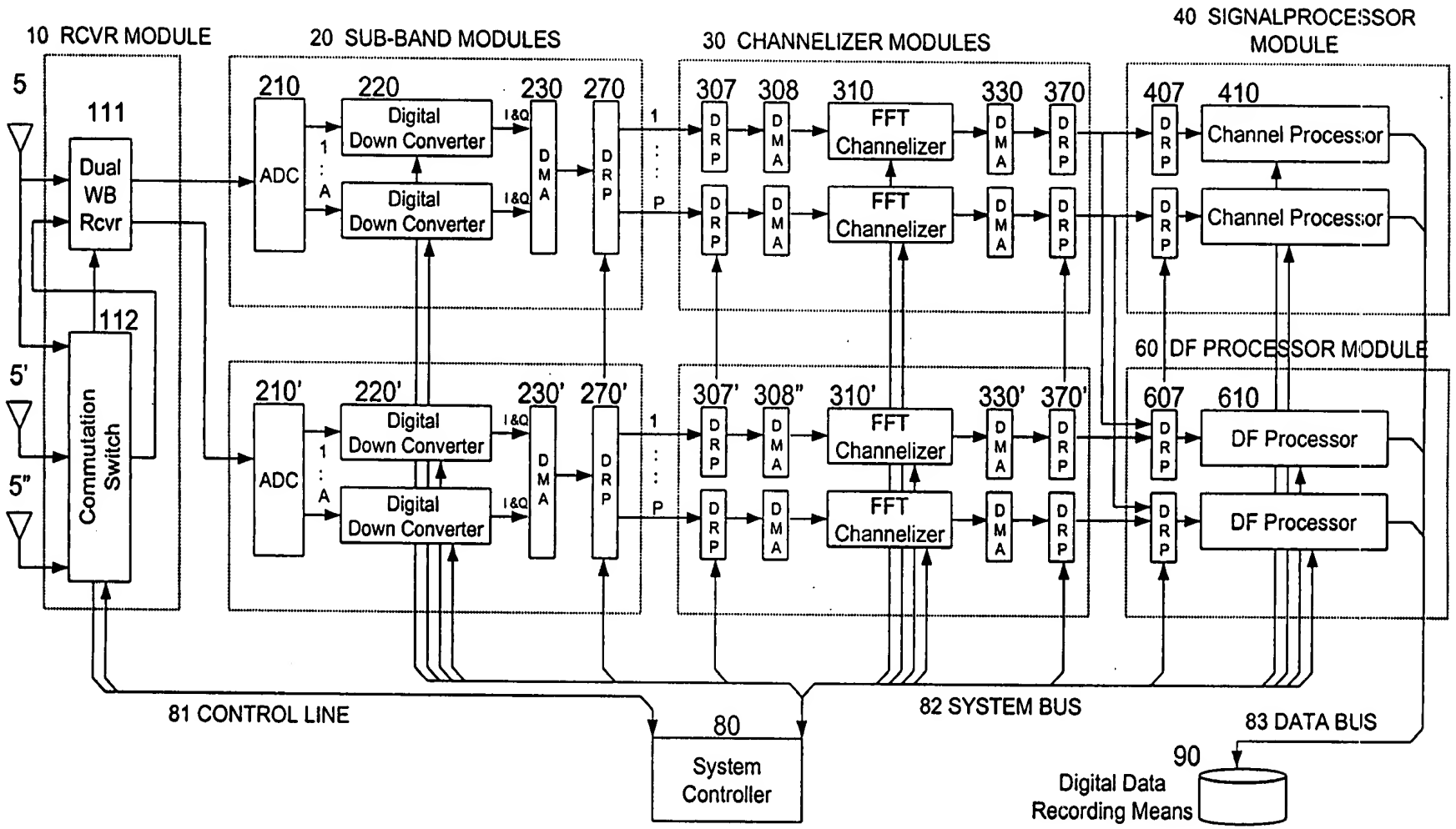

10 RCVR MODULE
20 SUB-BAND MODULES
30 CHANNELIZER MODULES
40 SIGNALPROCESSOR MODULE
60 DF PROCESSOR MODULE
5
5'
5"
111
112
Dual WB Rcvr
Commutation Switch
ADC
1 : A
210
210'
220
220'
Digital Down Converter
I&Q
230
230'
DMA
270
270'
DRP
1 : P
307
307'
308
308"
310
310'
FFT Channelizer
330
330'
370
370'
407
410
Channel Processor
607
610
DF Processor
81 CONTROL LINE
82 SYSTEM BUS
83 DATA BUS
80
System Controller
90
Digital Data Recording Means

Fig. 7

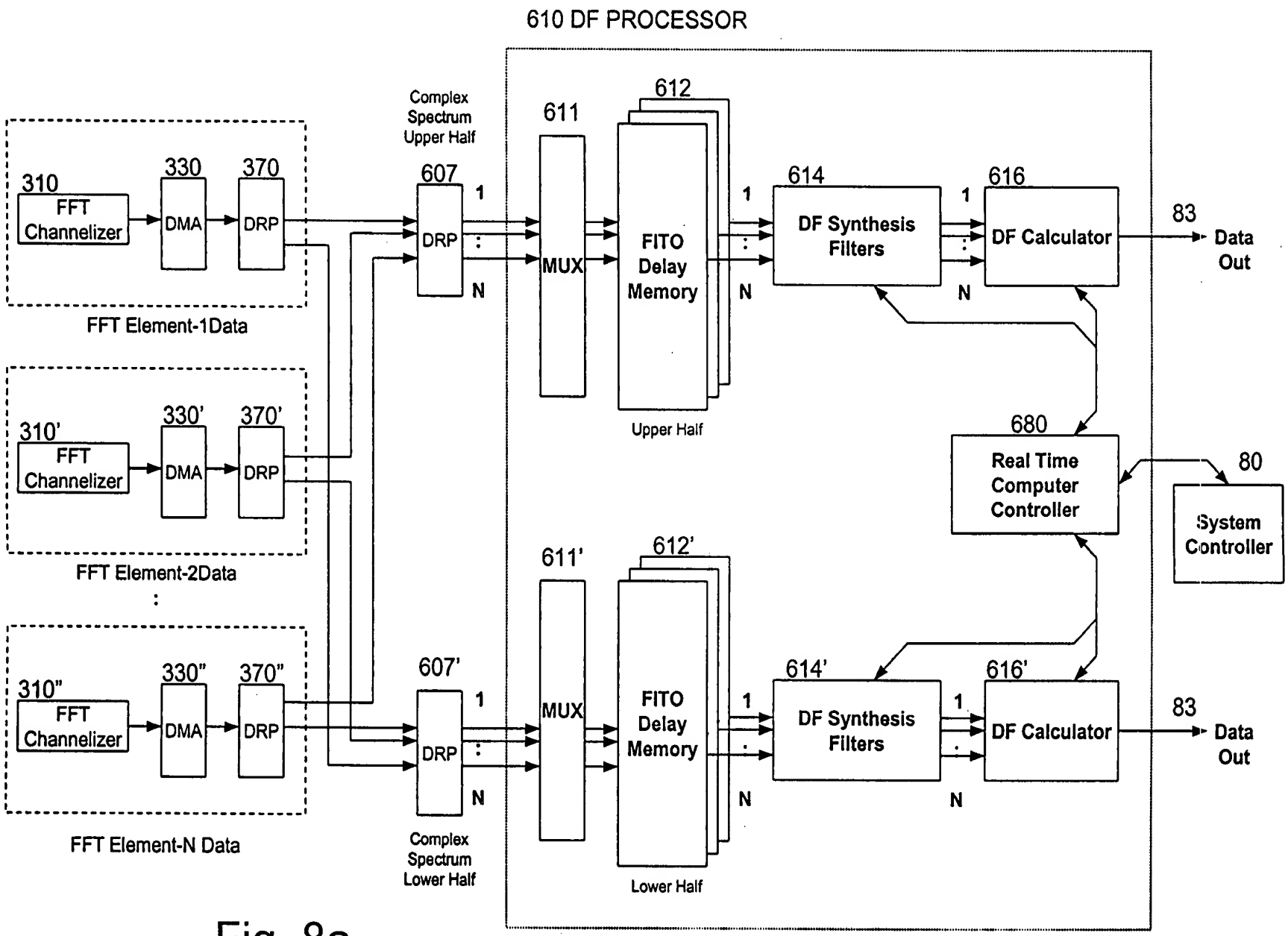
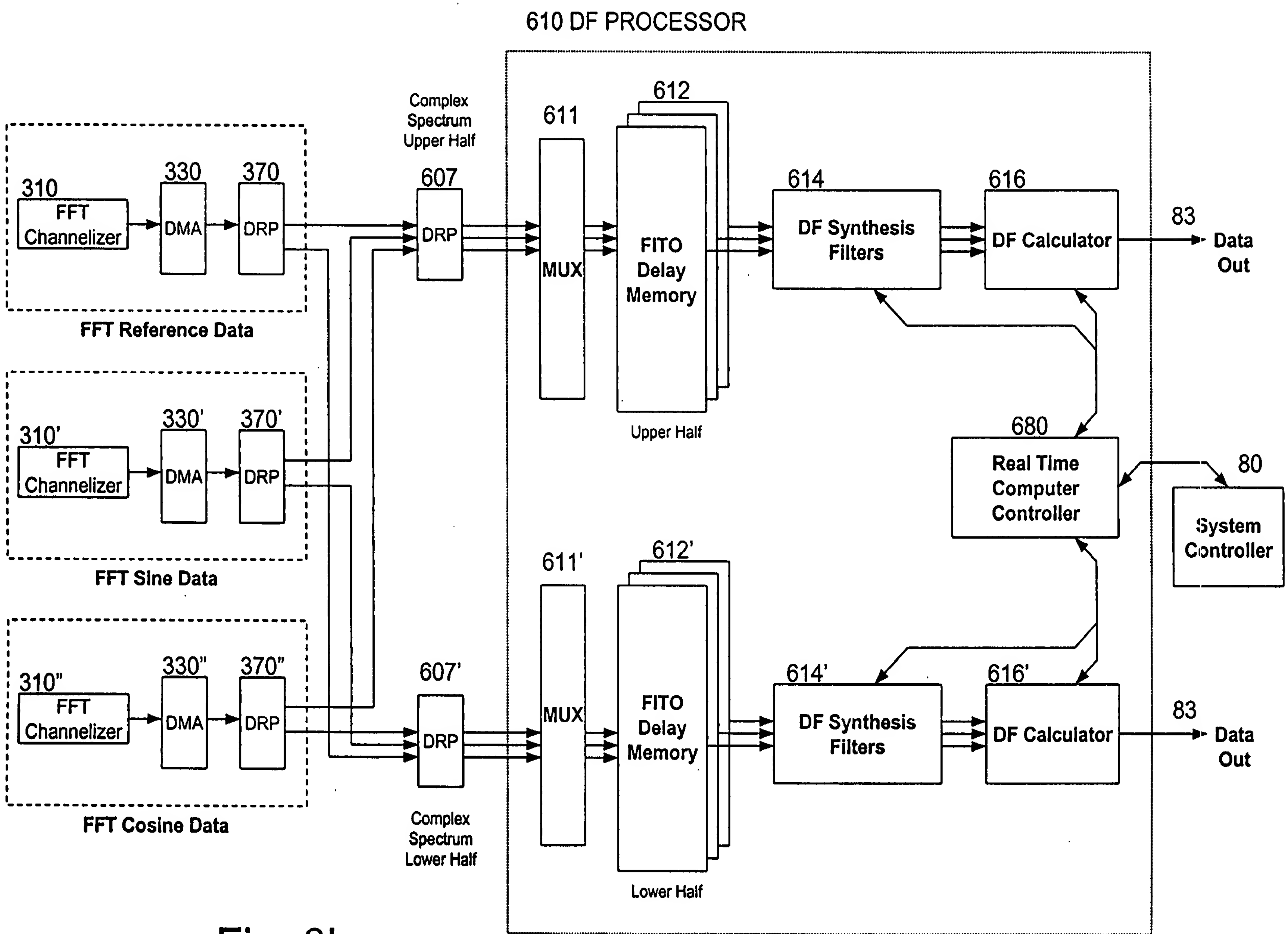


Fig. 8a



610 DF PROCESSOR
310
FFT
Channelizer
330
DMA
370
DRP
FFT Reference Data
310'
FFT
Channelizer
330'
DMA
370'
DRP
FFT Sine Data
310"
FFT
Channelizer
330"
DMA
370"
DRP
FFT Cosine Data
Complex
Spectrum
Upper Half
607
DRP
607'
DRP
Complex
Spectrum
Lower Half
611
MUX
612
FITO
Delay
Memory
Upper Half
611'
MUX
612'
FITO
Delay
Memory
Lower Half
614
DF Synthesis
Filters
616
DF Calculator
83
Data
Out
680
Real Time
Computer
Controller
80
System
Controller
614'
DF Synthesis
Filters
616'
DF Calculator
83
Data
Out

Fig. 8b

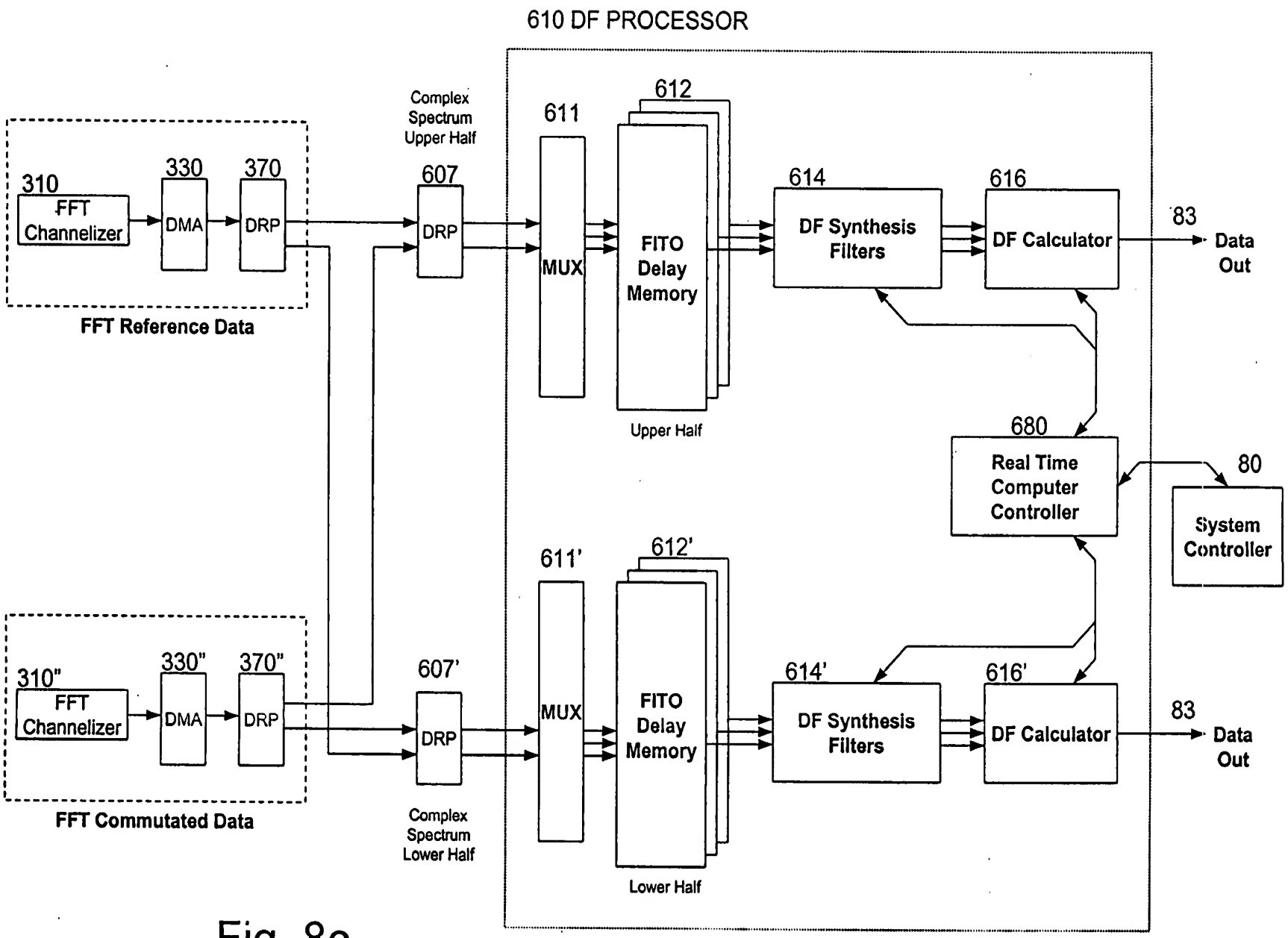

610 DF PROCESSOR
310
FFT Channelizer
330
DMA
370
DRP
FFT Reference Data
Complex Spectrum Upper Half
607
DRP
611
MUX
612
FITO Delay Memory
Upper Half
614
DF Synthesis Filters
616
DF Calculator
83
Data Out
680
Real Time Computer Controller
80
System Controller
310"
FFT Channelizer
330"
DMA
370"
DRP
FFT Commutated Data
607'
DRP
Complex Spectrum Lower Half
611'
MUX
612'
FITO Delay Memory
Lower Half
614'
DF Synthesis Filters
616'
DF Calculator
83
Data Out

Fig. 8c

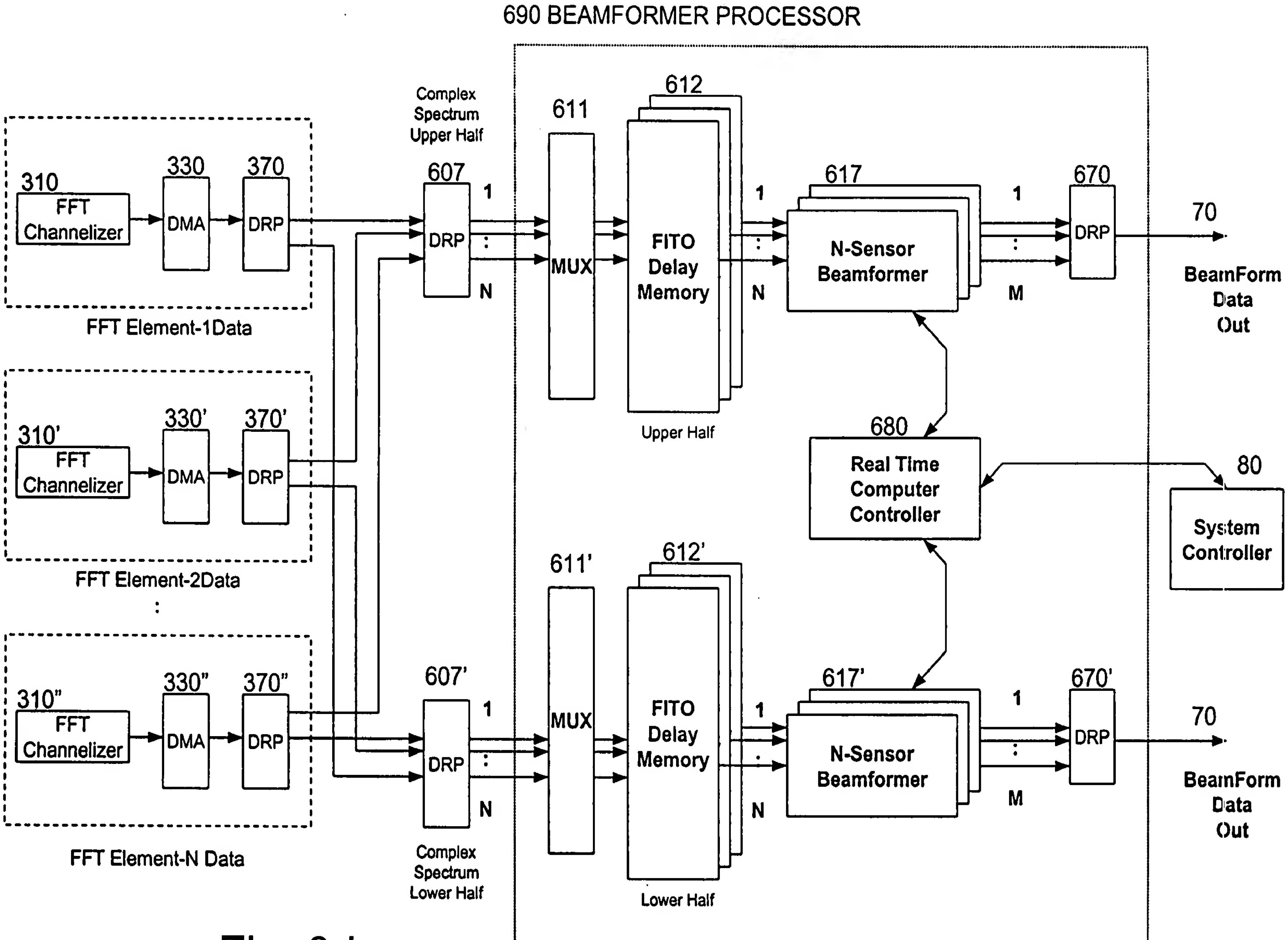

690 BEAMFORMER PROCESSOR
310
FFT Channelizer
330
DMA
370
DRP
FFT Element-1Data
310'
FFT Channelizer
330'
DMA
370'
DRP
FFT Element-2Data
:
310"
FFT Channelizer
330"
DMA
370"
DRP
FFT Element-N Data
Complex Spectrum Upper Half
607
DRP
1
:
N
607'
DRP
1
:
N
Complex Spectrum Lower Half
611
MUX
612
FITO Delay Memory
Upper Half
1
:
N
611'
MUX
612'
FITO Delay Memory
Lower Half
1
:
N
617
N-Sensor Beamformer
1
:
M
617'
N-Sensor Beamformer
1
:
M
680
Real Time Computer Controller
670
DRP
670'
DRP
70
BeamForm Data Out
70
BeamForm Data Out
80
System Controller

Fig. 8d

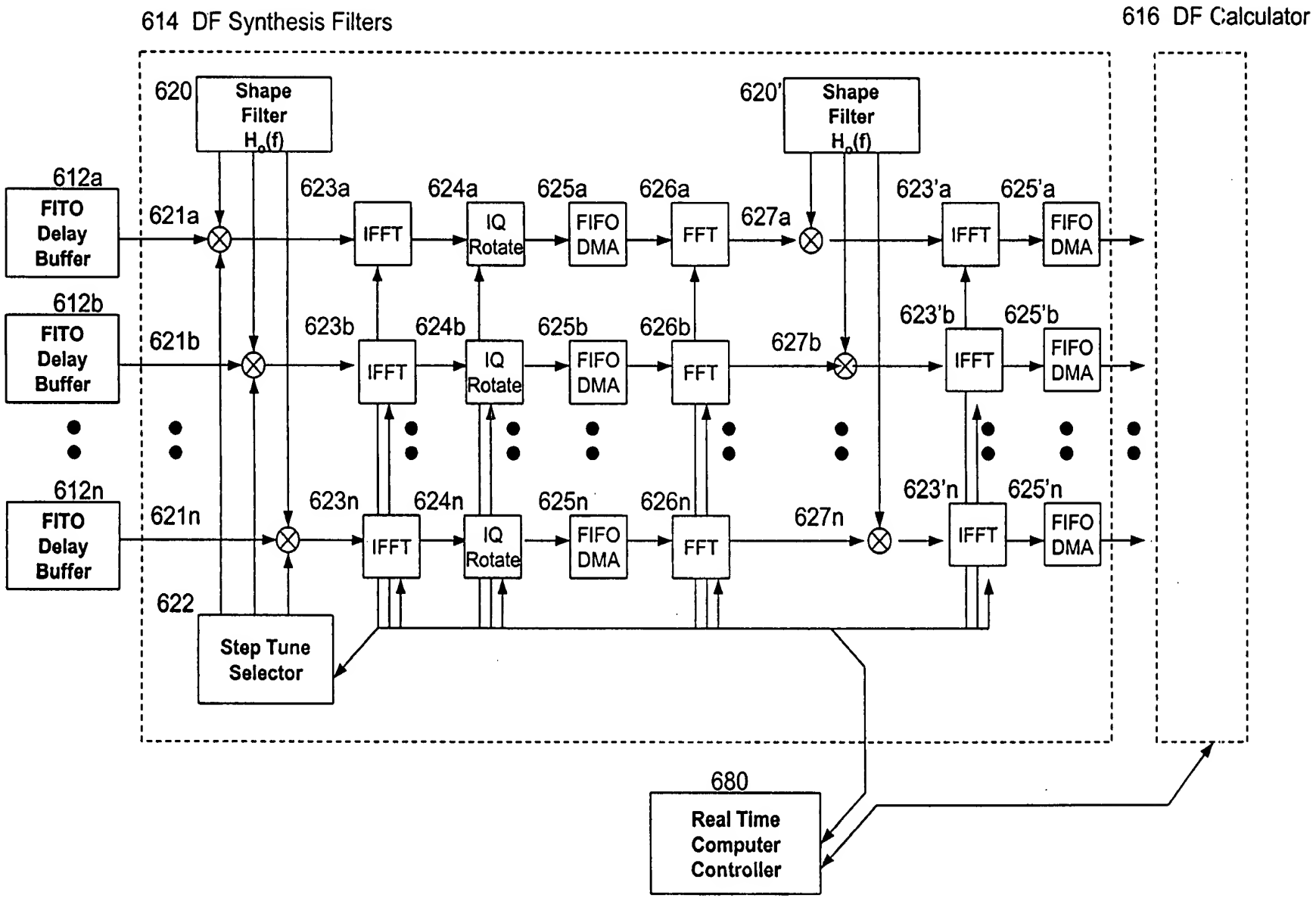

614 DF Synthesis Filters
616 DF Calculator
620
Shape Filter $H_o(f)$
620'
Shape Filter $H_o(f)$
612a
FITO Delay Buffer
612b
FITO Delay Buffer
612n
FITO Delay Buffer
621a
621b
621n
623a
623b
623n
624a
624b
624n
625a
625b
625n
626a
626b
626n
627a
627b
627n
623'a
623'b
623'n
625'a
625'b
625'n
IFFT
IQ Rotate
FIFO DMA
FFT
622
Step Tune Selector
680
Real Time Computer Controller

Fig. 9a

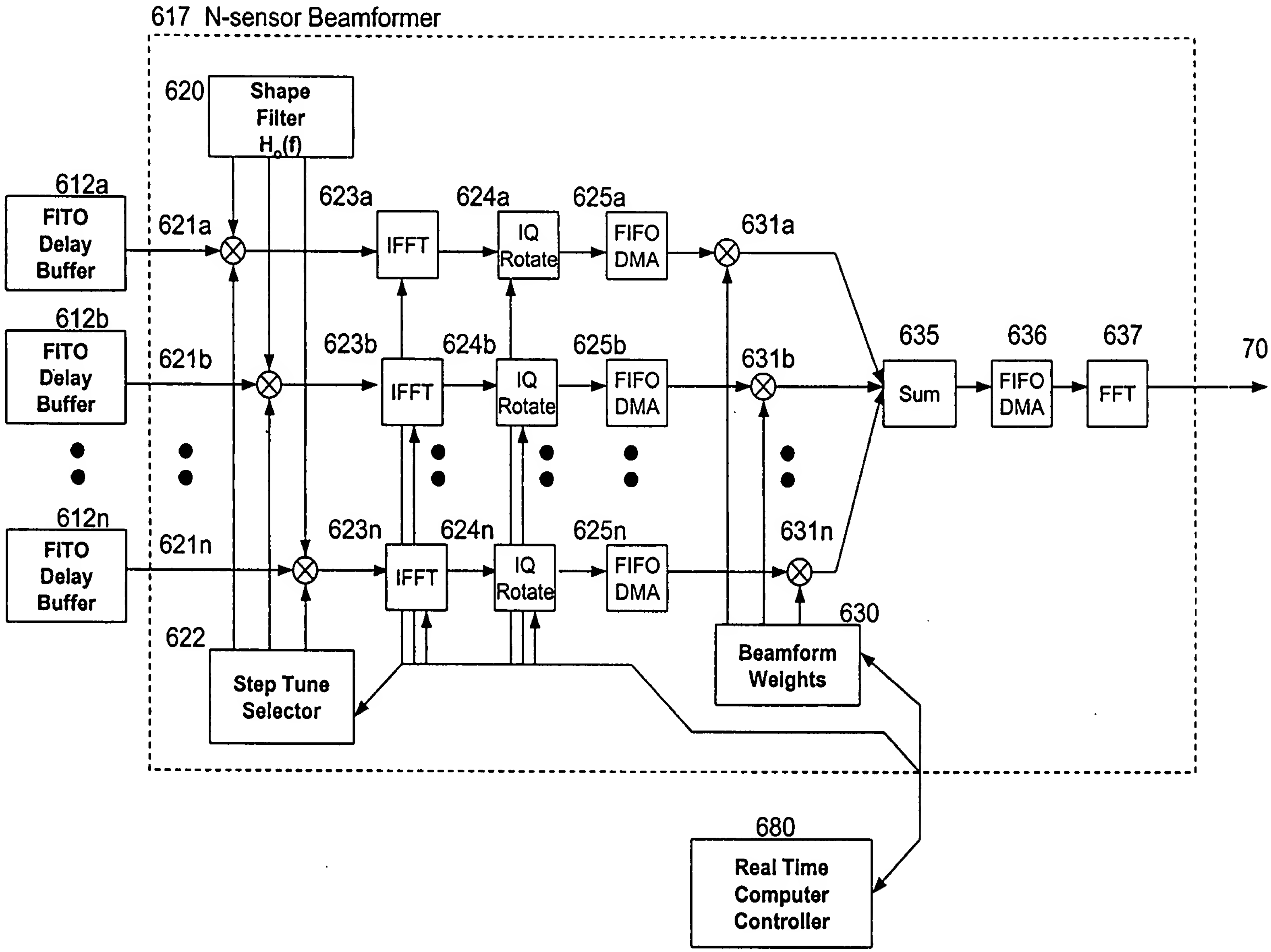

617 N-sensor Beamformer
620
Shape Filter $H_o(f)$
612a
FITO Delay Buffer
612b
FITO Delay Buffer
612n
FITO Delay Buffer
621a
621b
621n
622
Step Tune Selector
623a
623b
623n
IFFT
IFFT
IFFT
624a
624b
624n
IQ Rotate
IQ Rotate
IQ Rotate
625a
625b
625n
FIFO DMA
FIFO DMA
FIFO DMA
631a
631b
631n
630
Beamform Weights
635
Sum
636
FIFO DMA
637
FFT
70
680
Real Time Computer Controller

Fig. 9b

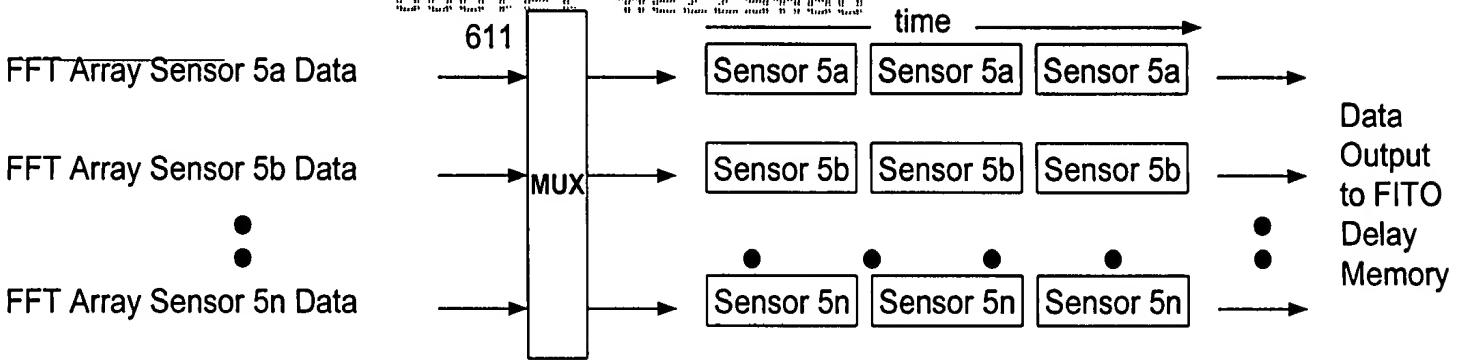


Fig. 10a

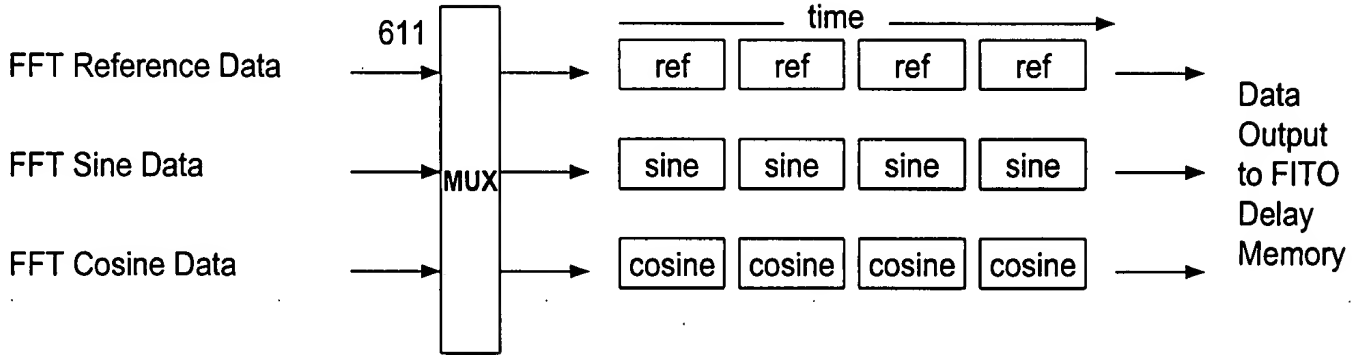


Fig. 10b

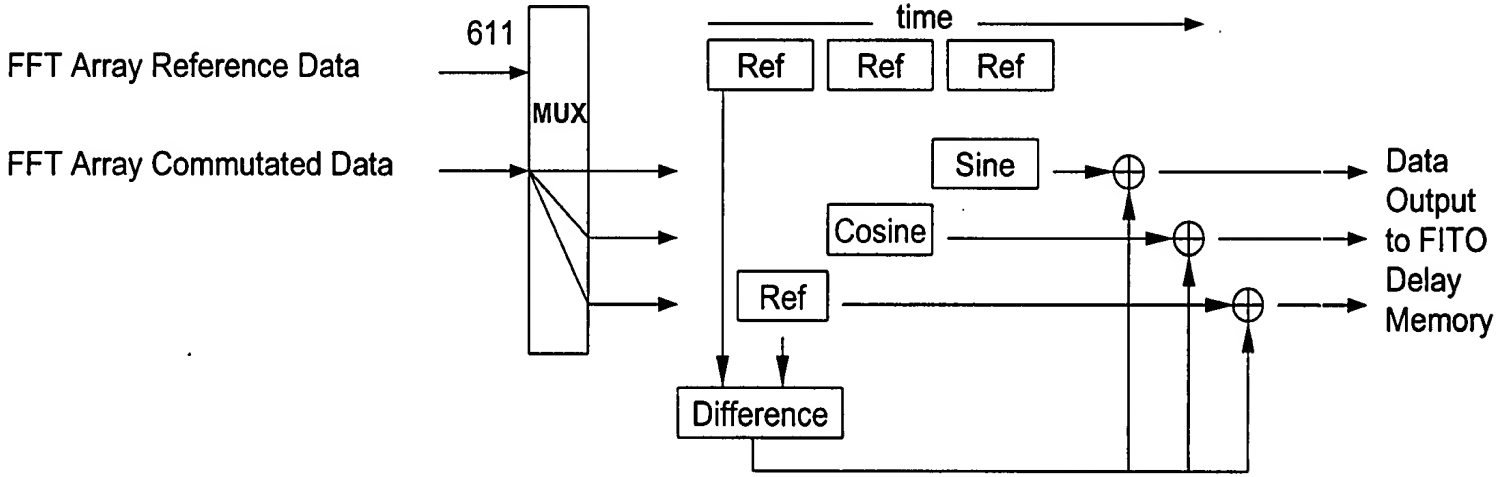


Fig. 10c

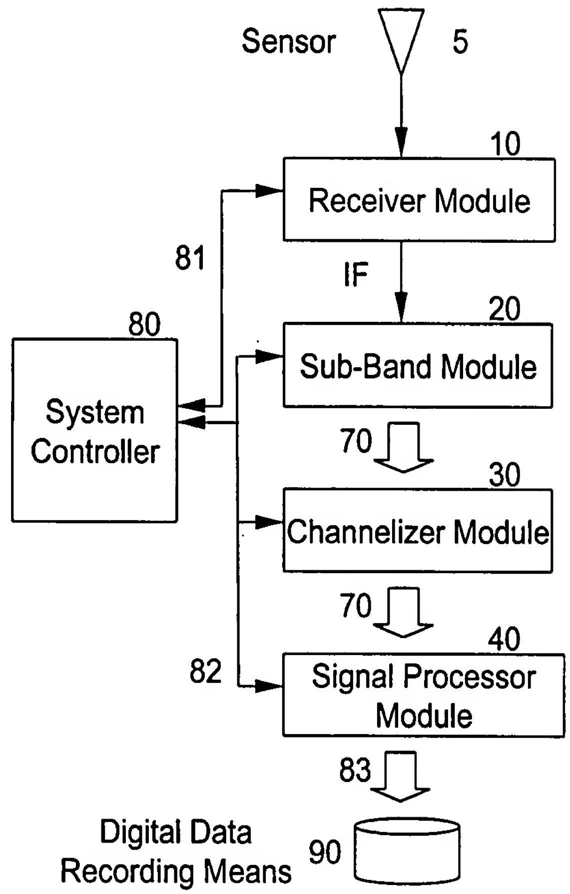

Sensor
5
10
Receiver Module
IF
81
80
20
Sub-Band Module
System
Controller
70
30
Channelizer Module
70
40
82
Signal Processor
Module
83
Digital Data
Recording Means
90

Fig. 11a

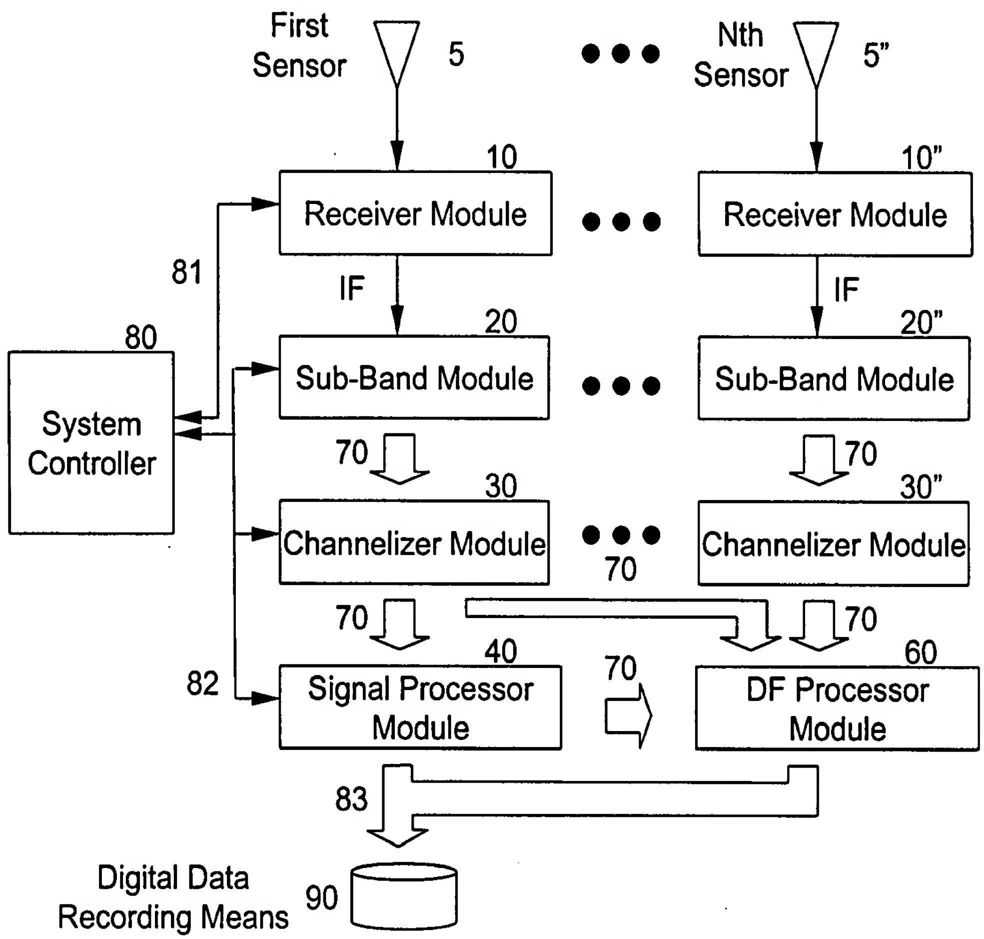

First Sensor
5
Nth Sensor
5"
10
Receiver Module
10"
Receiver Module
IF
IF
20
Sub-Band Module
20"
Sub-Band Module
80
System Controller
81
82
70
70
30
Channelizer Module
30"
Channelizer Module
70
70
70
40
Signal Processor Module
70
60
DF Processor Module
83
Digital Data Recording Means
90

Fig. 11b

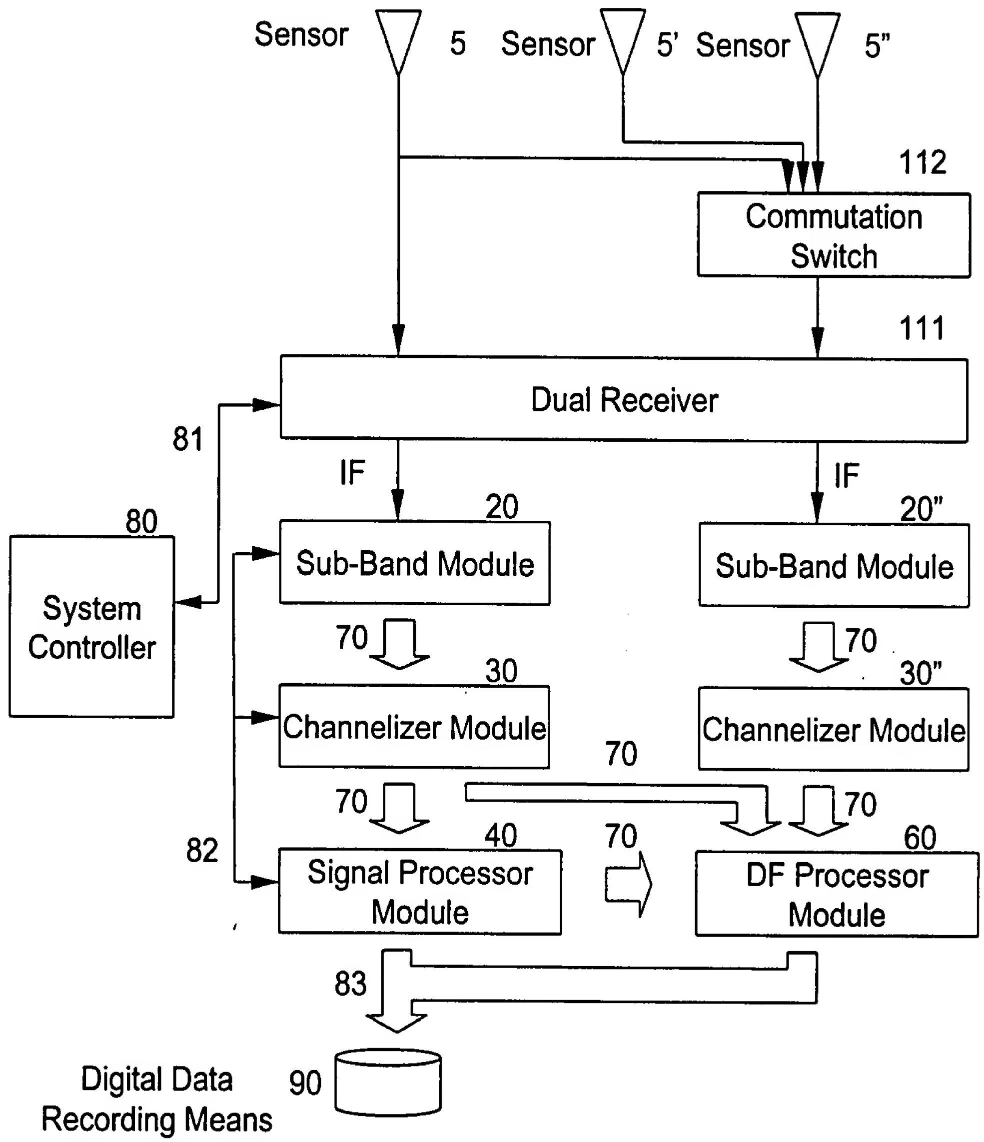

Sensor
5
Sensor
5'
Sensor
5"
112
Commutation Switch
111
Dual Receiver
81
IF
IF
80
System Controller
20
Sub-Band Module
20"
Sub-Band Module
70
70
30
Channelizer Module
30"
Channelizer Module
70
70
70
82
40
Signal Processor Module
70
60
DF Processor Module
83
Digital Data Recording Means
90

Fig. 11c

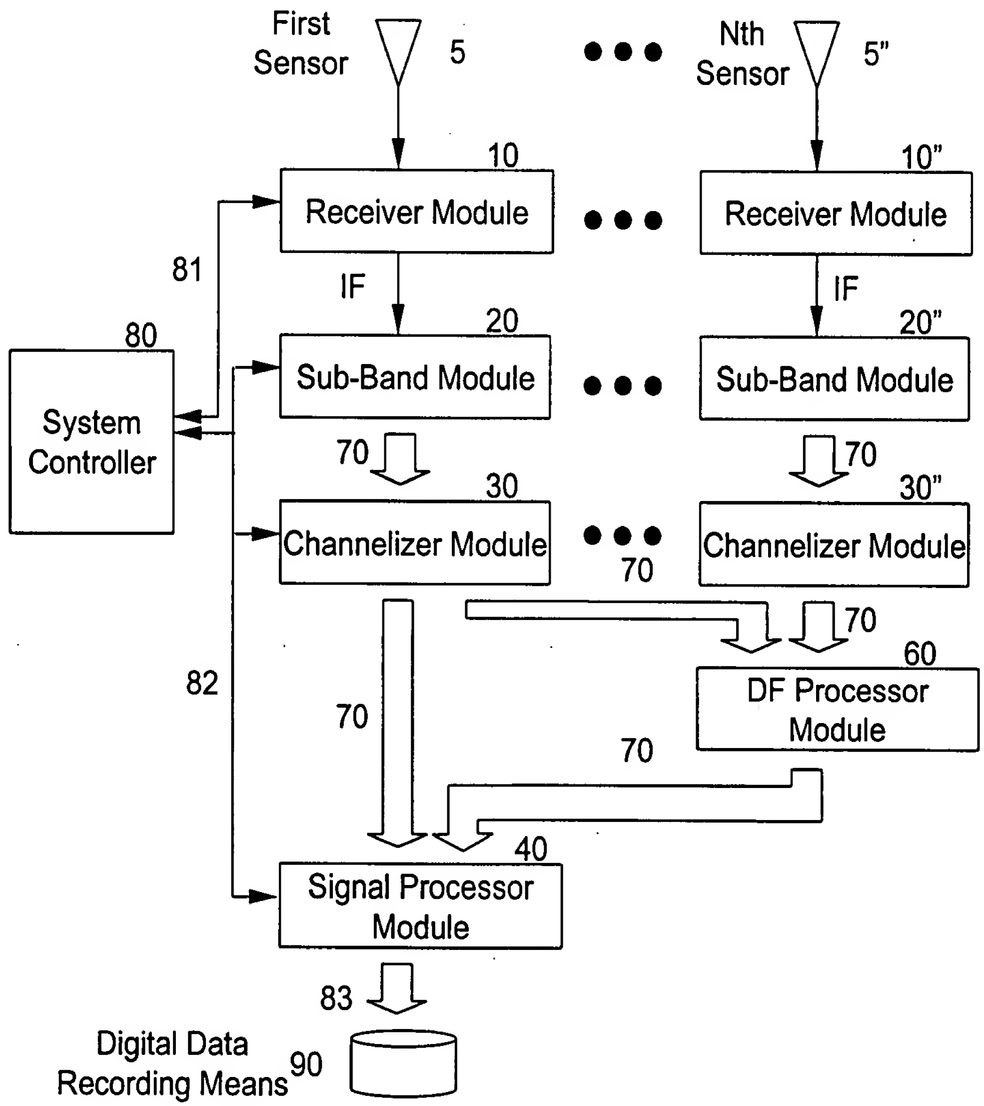


Fig. 11d

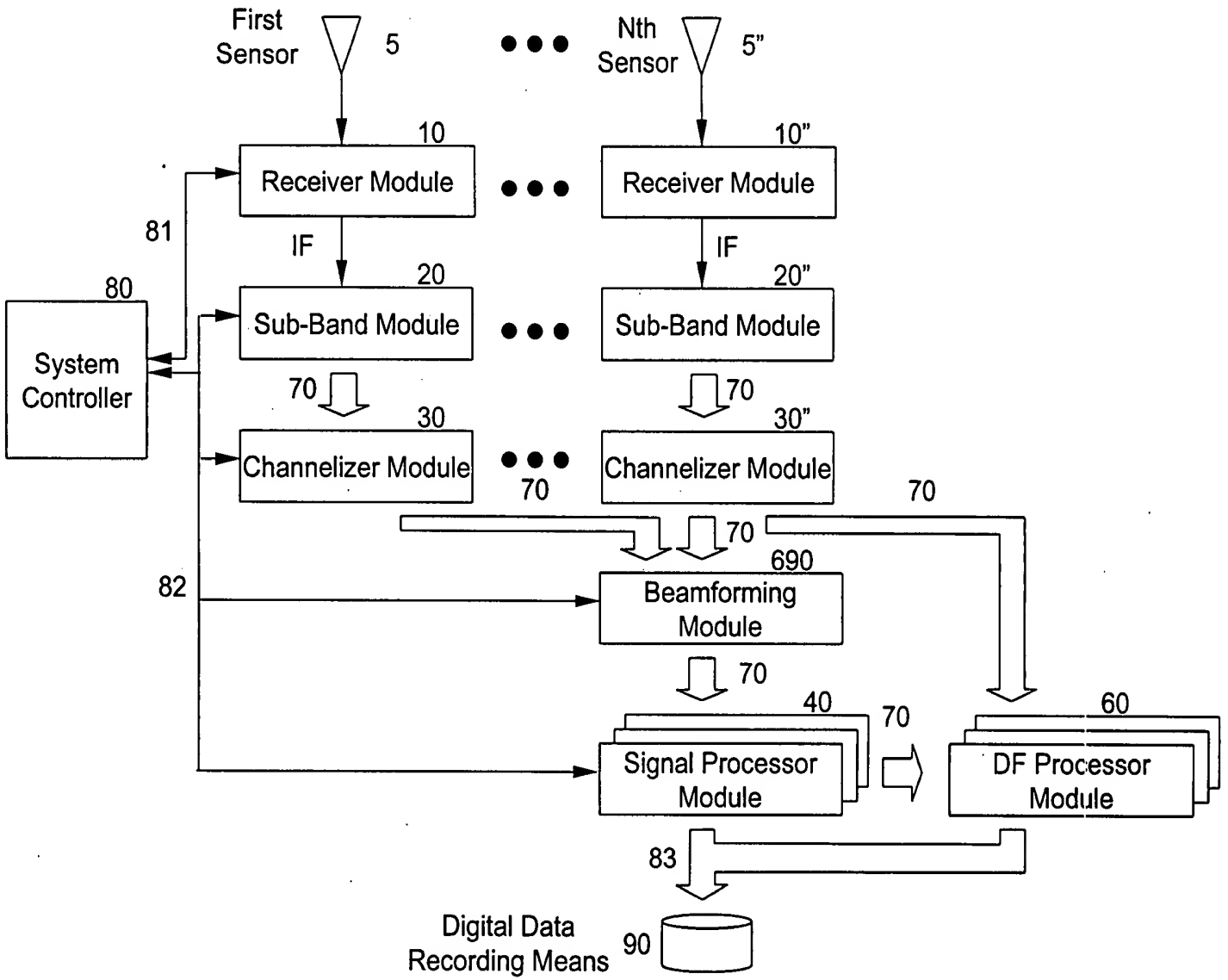

First Sensor
5
Nth Sensor
5"
10
Receiver Module
10"
Receiver Module
81
IF
IF
20
Sub-Band Module
20"
Sub-Band Module
80
System Controller
70
70
30
Channelizer Module
30"
Channelizer Module
70
70
70
690
82
Beamforming Module
70
40
70
60
Signal Processor Module
DF Processor Module
83
Digital Data Recording Means
90

Fig. 11e